REMARKS

Claims 26-28 were pending in the application. Claim 26 has been canceled in this paper. Claims 27-28 are now pending for examination.

Claims 26-28 were rejected under 35. U.S.C. § 112 for the use of the allegedly vague and indefinite terms "high-drain-withstand-voltage MOSFET" and "low-drain-withstand-voltage MOSFET." These terms have now been amended to "high withstand voltage MOSFET" and "low withstand voltage MOSFET", respectively, to overcome this objection. Applicants view this amendment as one of form only, and not as one that narrows the claims in any material way. Accordingly, no estoppel should arise from this amendment.

Claim 26 was rejected as being anticipated by the Haken patent (U.S. Patent No. 5,024,960). This rejection is now moot, as claim 26 has been canceled from the application in this paper.

Claim 27 was rejected under section 103 as being obvious in view of the Haken patent. Claim 27 has now been amended to depend from claim 28, for which the Examiner indicted allowable subject matter in the Office Action, and is thus believed to be patentable over the cited art.

The Examiner's indication of patentable subject matter in claim 28 is appreciated. Claim 28 has been rewritten in independent form to include all of its original limitations, along with the limitations of original claim 26 (which is now canceled, but from which claim 28 originally depended). Claim 28 should thus be patentable over the cited art, and the prompt allowance of claims 27 and 28 is now respectfully requested.

In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los

Angeles, California telephone number (213) 337-6700 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
HOGAN & HARTSON L.L.P.

Date: May 28, 2002

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Version with markings to show changes made:

27. (Amended) A semiconductor integrated circuit according to claim [26] 28, wherein the minimum gate length in the channel length direction of the LVMISFET is in the range of 1.5 – 2.5 μm.

28. (Amended) A semiconductor integrated circuit [according to claim 26, wherein the HVMISFET comprises] comprising:

an HVMISFET (high withstand voltage MOSFET) having:

a source region and drain region of a second conductivity type formed apart from each other on a surface of a semiconductor region of a first conductivity type,

a channel-forming region which is the surface of the semiconductor region between the source region and the drain region,

a gate formed on the channel-forming region via [the] a gate insulating film of a thickness in the range of 100 – 200 Å,

the drain region being constituted of a low concentration drain region and a high-concentration drain region in contact with each other,

the low-concentration drain region being disposed between the channel-forming region and the high concentration drain region, and

a field insulating film with a thickness at least one order of ten greater than that of the gate insulating film formed by self-alignment above the low-concentration drain region; and

an LVMISFET (low withstand voltage MOSFET) of the same conductivity type formed on the same semiconductor region and having the same threshold voltage and gate insulating film as the HVMISFET,

a surface concentration of the semiconductor region directly under the gate insulating film being partially increased to make the threshold voltage not less than 0.7 V and

drain regions and source regions of the HVMISFET and the LVMISFET being constituted as phosphorus impurity regions.